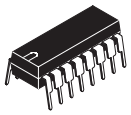


SLUS397A − JANUARY 2000 − REVISED AUGUST 2003

# LOW VOLTAGE DIFFERENTIAL (LVD) SCSI 9-LINE TERMINATOR

## FEATURES

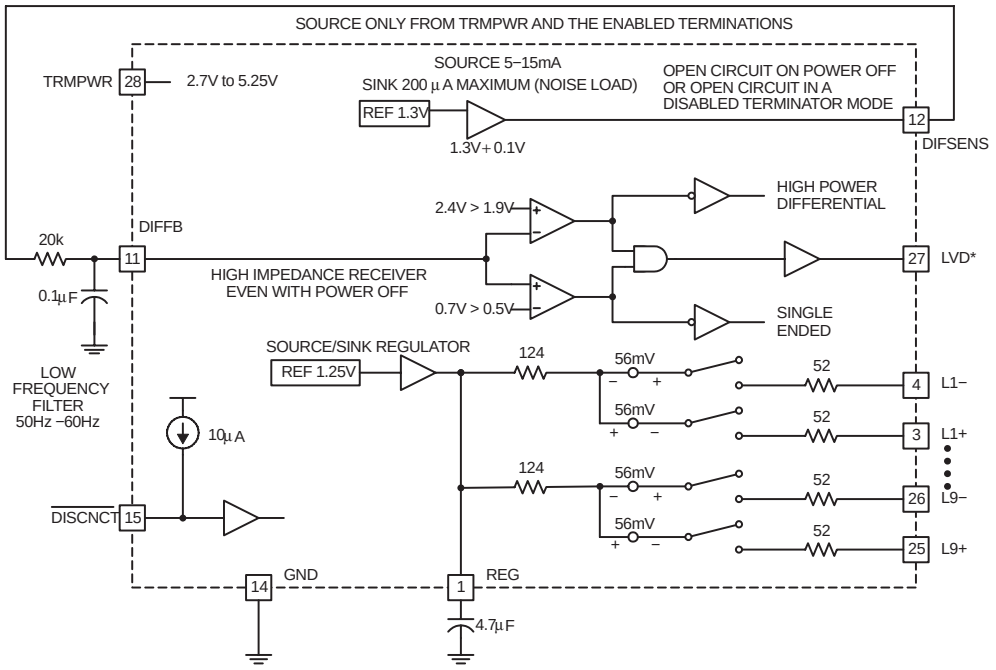
- **First LVD only Active Terminator**
- **Meets SCSI SPI−2 Ultra2 (Fast−40), SPI−3 Ultra3/Ultra160 (Fast−80) and SPI−4 Ultra320 (Fast−160) Standards**
- **2.7V to 5.25V Operation**
- **Differential Failsafe Bias**
- **Reversed Disconnect Polarity**

## DESCRIPTION

The UCC5641 is an active terminator for low voltage differential (LVD) small computer systems interface (SCSI) networks. This LVD only design allows the user to reach peak bus performance while reducing system cost. The device is designed as an active Y-terminator to improve the frequency response of the LVD bus. Designed with a 1.5-pF channel capacitance, the UCC5641 allows for minimal bus loading for a maximum number of peripherals. With the UCC5641, the designer will be able to comply with the Fast-40 SPI-2, Fast-80 SPI-3 and Fast-160 SPI-4 specifications. The UCC5641 also provides a much-needed system migration path for ever improving SCSI system standards. This device is available in the 24-pin and 28-pin TSSOP for ease of layout use.

The UCC5641 is not designed for use in single ended (SE) or high voltage differential (HVD) systems.

## BLOCK DIAGRAM




These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

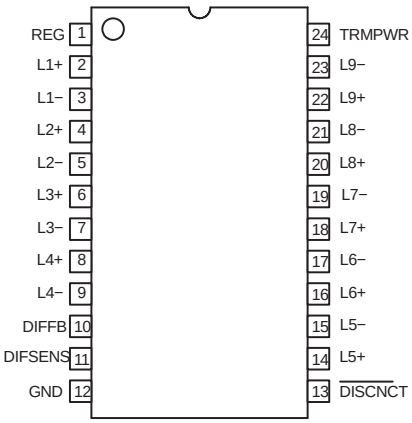
## ORDERING INFORMATION

| $T_A$ | PACKAGED DEVICE† | |
|---|---|---|
| | TSSOP-24 (PWP) | TSSOP-28 (PWP) |
| 0°C to 70°C | UC5641PW24 | UC5641PW28 |

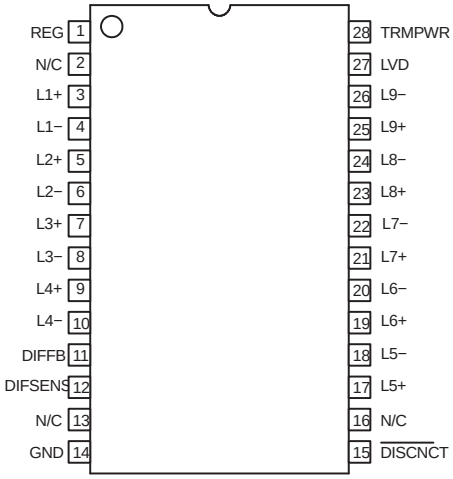
† The TSSOP packages are available taped and reeled. Add TR suffix to device type (e.g. UC5641PW24TR) to order quantities of 2,000 devices per reel.

## CONNECTION DIAGRAM

**TSSOP-24 (Top View)**
**PW Package**




**TSSOP-28 (Top View)**
**PW Package**




## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| TRMPWR voltage | 2.7 | | 5.25 | V |
| Signal line voltage | 0 | | 5.0 | |
| Disconnect input voltage | 0 | | TRMPWR | °C |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted†‡

| PARAMETER | UCC5641 | UNIT |
|---|---|---|
| TRMPWR voltage | 6 | V |
| Signal line voltage | 0 to 3.6 | |
| Package dissipation | 1 | W |
| Storage temperature, $T_{stg}$ | −65 to 150 | °C |
| Operating junction temperature, $T_J$ | –55 to 150 | |
| Lead temperature (soldering, 10 sec.) | 300 | |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into and negative out of, the specified terminal.

‡ Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

## ELECTRICAL CHARACTERISTICS

specifications apply for TA = 05C to 705C, TRMPWR = 3.3V. TA = TJ. (Unless otherwise stated)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **TRMPWR Supply Current Section** | | | | | |
| TRMPWR supply current | No load | | | 25 | mA |
| | Disabled terminator | | | 400 | µA |
| TRMPWR voltage | | 2.7 | | 5.25 | V |
| **Regulator Section** | | | | | |
| 1.25-V regulator | DIFSENS connected to DIFFB | 1.15 | 1.25 | 1.35 | V |
| 1.25-V regulator source current | DIFSENS connected to DIFFB | | –100 | –80 | mA |
| 1.25-V regulator sink current | DIFSENS connected to DIFFB | 80 | 100 | | |
| 1.3-V regulator | DIFFB connected to GND | 1.2 | 1.3 | 1.4 | V |
| 1.3-V regulator source current | DIFSENS to GND | –15 | | –5 | mA |
| 1.3-V sink current | DIFSENS to 3.3 V | 50 | | 200 | µA |
| **Differential Termination Section** | | | | | |
| Differential impedance | –2.5 mA to 4.5 mA | 100 | 105 | 110 | Ω |
| Common mode impedance | L+ connected to L– | 110 | 150 | 165 | |
| Differential bias voltage | No load, L+ or L– | 100 | | 125 | mV |
| Common mode bias | | 1.15 | 1.25 | 1.35 | V |
| Output leakage, disconnect | DISCNCT, TRMPWR = 0 V to 5.25 V, $V_{LINE}$ = 0.2 V to 5.25 V | | 10 | 400 | nA |
| Output capacitance | Single ended measurement to ground(1) | | | 3 | pF |
| **Low Voltage Differential (LVD) Status Bit Section** | | | | | |
| $I_{SOURCE}$ | $V_{LOAD}$ = 2.4 V | | –6 | –4 | mA |
| $I_{SINK}$ | $V_{LOAD}$ = 0.4 V | 2 | 5 | | |
| **Disconnect & Differential Sense Input Section** | | | | | |
| $\overline{\text{DISCNCT}}$ threshold | | 0.8 | | 2 | V |
| Input current | At 0 V and 3.3 V | –30 | –10 | | µA |
| Differential sense SE to LVD threshold | | 0.5 | | 0.7 | V |
| Differential sense LVD to HPD threshold | | 1.9 | | 2.4 | |

NOTE: (1) Ensured by design. Not production tested.

## TERMINAL FUNCTIONS(1)

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| DIFFB | 14 | I | Differential sense filter pin should be connected to a 4.7-µF capacitor and 50-kΩ resistor to Diff Sense. |
| DIFSENS | 14 | O | The SCSI bus differential sense line to detect what type of devices are connected to the SCSI Bus. |
| $\overline{\text{DISCNCT}}$ | 6 | I | Disconnect pin shuts down the terminator when it is not at the end of the bus. |
| GND | 5 | | Ground reference for the device |
| Ln− | 14 | | Negative line in differential applications for the SCSI Bus. |
| Ln+ | 14 | | Positive line for differential applications for the SCSI Bus. |
| LVD | 14 | O | 28-pin package only. Indicates that the bus is in LVD mode. |
| REG | 14 | | Regulator bypass; must be connected to a 4.7-µF capacitor to ground. |
| TRMPWR | 11 | | $V_{IN}$ 2.7-V to 5.25-V supply, bypass near the terminators with a 4.7-µF capacitor to ground. |

NOTE: (1) PWP package.

## APPLICATION INFORMATION

All SCSI buses require a termination network at each end to function properly. Specific termination requirements differ, depending on which types of SCSI driver devices are present on the bus. The UCC5641 is a low-voltage differential (LVD)-only device. It senses which types of drivers are present on the bus. If it detects the presence of a single-ended (SE) or high-voltage differential (HVD) driver, the UCC5641 will place itself in a high-impedance input state, effectively disconnecting the chip from the bus.

The UCC5641 senses what kinds of drivers are present on the bus by the voltage on SCSI bus control line DIFFSENS, which is monitored by the DIFFB input pin. The DIFSENS output pin on the UCC5641 attempts to drive a DIFFSENS control line to 1.3 V. If only LVD devices are present, the DIFFSENS line will be successfully driven to that voltage. If HVD drivers are present, they will pull the DIFFSENS line high. If any single-ended drivers are present, they pull the DIFSENS line to ground (even if HVD drivers are also present on the bus). If the voltage on the DIFFB is below 0.5 V or above 2.4 V, the UCC5641 enters the high-impedance SE/HVD state. If it is between 0.7 V and 1.9 V, the UCC5641 enters the LVD mode. These thresholds accommodate differences in ground potential that can occur between the ends of long bus lines.

Three UCC5641 devices are required at each end of the SCSI bus to terminate 27 lines (18 data, 9 control). Every UCC5641 contains a DIFSENS driver, but only one should be used to drive the line at each end. The DIFSENS pin on the other devices should be left unconnected.

On power up (the voltage on the TRMPWR pin rising above 2.7 V), the UCC5641 assumes the SE/HVD mode.

The DIFFB inputs on all three chips at each end of the bus should be connected together. Properly filtered, noise on DIFFB will not cause a false mode change. There should be a shared 50-Hz noise filter implemented on DIFFB at each end of the bus as close as possible to the DIFFB pins. This is implemented with a 50-kΩ resistor between the DIFFB and DIFSENS pins, and a 4.7-μF capacitor from DIFFB to ground. See the *Typical Application* diagram at the end of this datasheet.

In LVD mode, the regulated voltage is switched to 1.25 V and a resistor network is presented to each line pair that provides common-mode impedance of 150 Ω and differential impedance of 105 Ω. The lines in each differential pair are biased so that when not driven, Line(n)+ and Line(n)− are driven 56 mV below and above the common-mode bias voltage (1.25 V) respectively.

In SE/HVD mode, all the terminating resistors are switched off the bus. The 1.25-V and 1.3-V (DIFSENS) regulators are left on.

When the disconnect input (DISCNCT) is active (high), the terminating resistors are switched off the bus and both voltage regulators are turned off to save power. The mode change filter/delay function is still active and the LVD pin (in the 28-pin package) continues to indicate the correct bus mode.

The UCC5641 operates down to a TRMPWR voltage of 2.7 V. This accommodates a 3.3-V system with allowance for supply tolerance (±10%), a unidirectional fusing device, and cable drop. The UCC3912 or UCC3918 is recommended for 3.3-V systems and the UCC3916 is recommended for 5-V systems in place of a fuse and diode implementation, as its lower voltage drop provides additional voltage margin for the system.

## APPLICATION INFORMATION

Layout is important in all SCSI implementations and critical in SPI-2, SPI-3 and SPI-4 systems, which have stringent requirements on both the absolute value of capacitance on differential signal lines and the balancing of capacitance between paired lines and from pair to pair.

Feedthroughs, through-hole connections, and etch lengths need to be carefully balanced. Standard multilayer power and ground plane spacing adds about 1 pF to each plane. Each feed-through will add 2.5 pF to 3.5 pF. Enlarging the clearance holes on both power and ground planes reduces capacitance. Opening up the power and ground planes under a through-hole connector reduces added capacitance in those applications. Capacitance is also affected by components in close proximity on both sides of the board.

### Maximum Capacitance

| SCSI Class | Trace to GND: REQ, ACK, DATA, Parity, P_CRCA | Trace to Trace: REQ, ACK, DATA, Parity, P_CRCA | Trace to GND: Other signals | Trace to Trace: Other Signals |
|---|---|---|---|---|
| **Ultra1** | 25 pF | N/A | 25 pF | N/A |
| **Ultra2** | 20 pF | 10 pF | 25 pF | 13 pF |
| **Ultra3/Ultra160** | 15 pF | 8 pF | 25 pF | 13 pF |
| **Ultra320** | 13 pF | 6.5 pF | 21 pF (est.) | 10 pF (est.) |

TI terminators are designed with very tightly controlled capacitance on their signal lines. Between the positive and negative lines in a differential pair the difference is typically no more than 0.1 pF, and only 0.3 pF between pairs.

Multi-layer boards need to adhere to the 120-Ω impedance standard, including the connector and feedthroughs. Bus traces are normally run on the outer layers of the board with 4-mil etch and 4-mil spacing between the two lines in each differential pair, and a minimum of 8-mil spacing to adjacent pairs to minimize crosstalk. Microstrip technology is too low in impedance and should not be used, it is designed for 50 Ω rather than 120-Ω differential systems.

Decoupling capacitors should be installed as close as possible to the following input pins of the UCC5641:

TRMPWR: 4.7-µF capacitor to ground, 0.01-µF capacitor to ground (high-frequency, low ESR)

REG: 4.7-µF capacitor to ground, 0.01-µF capacitor to ground (high-frequency, low ESR)

## APPLICATION INFORMATION

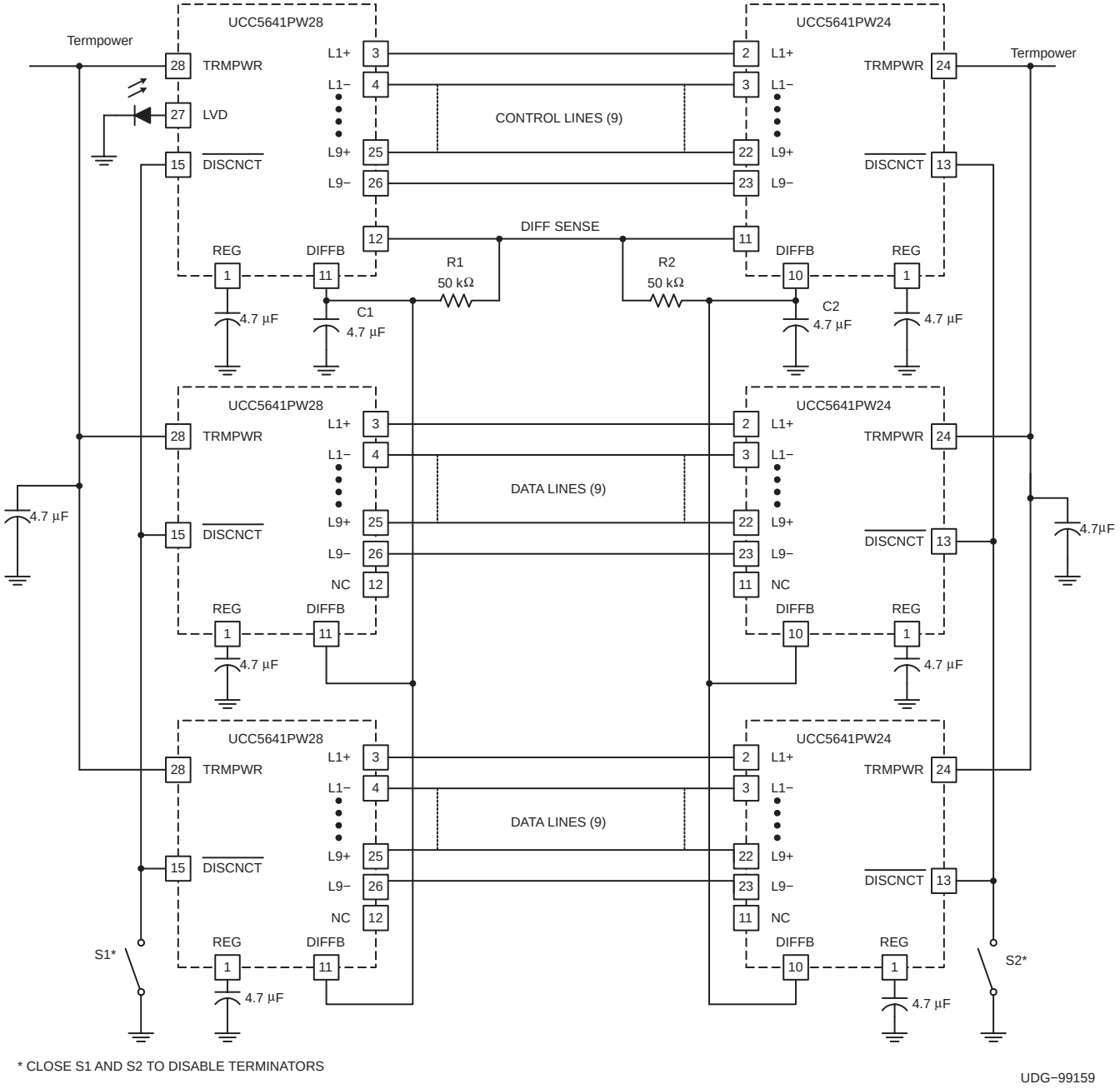



**Figure 1. Typical Application Diagram**

**Table 1. Component Slection**

| STANDARD | R1, R2 | C1, C2 |
|---|---|---|
| SPI−2 | 20 kΩ | 0.1 µF |
| SPI−3, 4 | 50 kΩ | 4.7 µF |

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| **Products** | | **Applications** | |
|---|---|---|---|
| Amplifiers | amplifier.ti.com | Audio | www.ti.com/audio |
| Data Converters | dataconverter.ti.com | Automotive | www.ti.com/automotive |
| DSP | dsp.ti.com | Broadband | www.ti.com/broadband |
| Interface | interface.ti.com | Digital Control | www.ti.com/digitalcontrol |
| Logic | logic.ti.com | Military | www.ti.com/military |
| Power Mgmt | power.ti.com | Optical Networking | www.ti.com/opticalnetwork |
| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
| | | Telephony | www.ti.com/telephony |
| | | Video & Imaging | www.ti.com/video |
| | | Wireless | www.ti.com/wireless |

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265